WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, the method comprising:

forming an opening in an upper surface of a porous low-k dielectric layer;

filling the opening with copper (Cu) or a Cu alloy;

conducting chemical-mechanical polishing (CMP) leaving this upper surface of the Cu or Cu alloy exposed; and

treating the upper surface of the Cu or Cu alloy with a plasma while controlling plasma conditions to avoid etching the upper surface of the porous low-k material.

2. The method according to claim 1, further comprising depositing a capping layer on the treated upper surface of the Cu or Cu alloy.

3. The method according to claim 2, comprising depositing silicon nitride or silicon carbide as the capping layer.

4. The method according to claim 1, comprising treating the upper surface of the Cu or Cu alloy in an ammonia (NH_3) or hydrogen (H_2) plasma.

5. The method according to claim 4, comprising treating the upper surface of the Cu or Cu alloy with the plasma at a power of 75 to 125 watts.

6. The method according to claim 5, comprising treating the upper surface of the Cu or Cu alloy with the plasma for 2 to 8 seconds.

7. The method according to claim 4, comprising treating the upper surface of the Cu or Cu alloy with a plasma for 2 to 8 seconds.

8. The method according to claim 4, comprising treating the upper surface of the Cu or Cu alloy with an NH_3 plasma at:

an NH_3 flow rate of 100 to 700 sccm;

a nitrogen (N_2) flow rate of 2,000 to 9,000 sccm;

a power of 35 to 125 watts;

a pressure of 4.0 to 5.2 torr; and

a temperature of 300° C to 400° C; for

2 to 8 seconds.

9. The method according to claim 4, comprising treating the upper surface of the Cu or Cu alloy with an H_2 plasma at:

a H_2 flow rate of 100 to 400 sccm;

an N_2 flow rate of 200 to 8,000 sccm;

a power of 75 to 125 watts;

a pressure of 4.0 to 5.2 torr; and

a temperature of 300° C to 400° C; for

2 to 8 seconds.

10. The method according to claim 4, comprising forming the opening in a dielectric layer having a dielectric constant (k) up to 2.4.

11. The method according to claim 10, comprising forming the opening in a dielectric layer having a k value of 2.0 to 2.2.

12. The method according to claim 4, comprising forming the opening as a dual damascene opening.

13. The method according to claim 1, comprising depositing a barrier metal layer lining the opening before filling the opening with the Cu or the Cu alloy.

14. The method according to claim 13, comprising depositing tantalum, tantalum nitride, or a composite of tantalum nitride and alpha (α)-tantalum, as the barrier metal layer.

15. A method of fabricating a semiconductor device, the method comprising:

forming a dual damascene opening in an upper surface of a porous dielectric layer having a dielectric constant (k) up to 2.4;

depositing a barrier metal layer lining the opening;

filling the opening with copper (Cu) or a Cu alloy;

conducting chemical-mechanical polishing (CMP) leaving an upper surface of the Cu or Cu alloy exposed;

treating the exposed upper surface of the Cu or Cu alloy in an ammonia (NH_3) or a hydrogen (H_2) plasma at a power of 75 to 125 watts for 2 to 8 seconds; and

depositing a capping layer.

16. The method according to claim 15, comprising treating the exposed upper surface of the Cu or Cu alloy in the plasma at:

an NH_3 flow rate of 100 to 700 sccm;

a nitrogen (N_2) flow rate of 2,000 to 9,000 sccm;

a pressure of 4.0 to 5.2 torr; and

at a temperature of 300° C to 400° C.

17. The method according to claim 15, comprising treating the exposed upper surface of the Cu or Cu alloy with the plasma at:

a H_2 flow rate of 100 to 400 sccm;

a nitrogen (N_2) flow rate of 200 to 8,000 sccm;

a pressure of 4.0 to 5.2 torr; and

a temperature of 300° C to 400° C.

18. The method according to claim 15, comprising forming the opening in a dielectric layer have a k value of 2.0 to 2.2.

19. A method according to claim 15, comprising depositing silicon nitride or silicon carbide as the capping layer.

20. The method according to claim 15, comprising depositing a layer of tantalum, tantalum nitride, or a composite of tantalum nitride and alpha (α)-tantalum, as the barrier metal layer.